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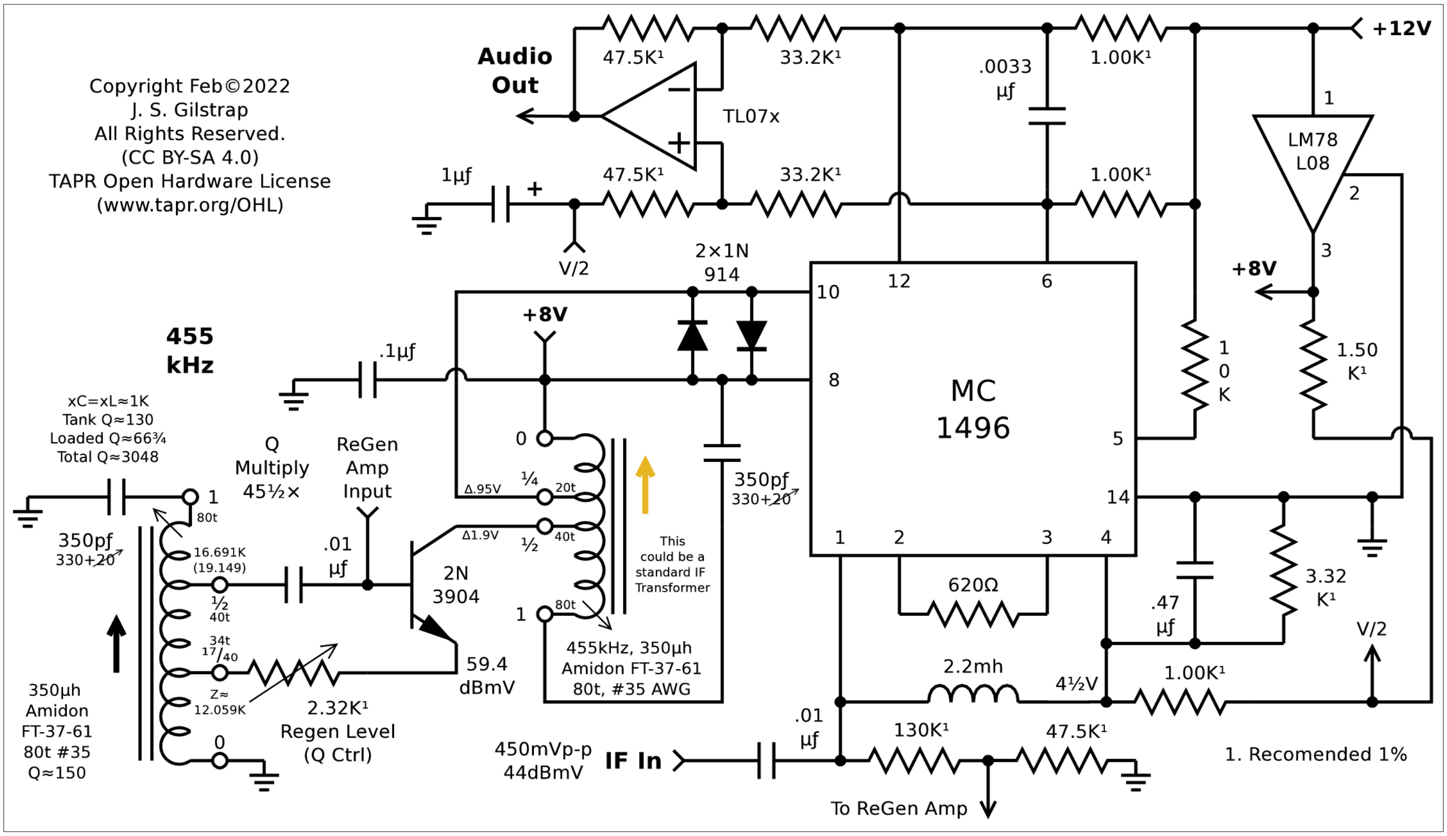
QuasiSync™ AM

A Regenerative BFO & Gated Semi-Synchronous AM Detector



Synchronous detection uses a PLL and a lock detection circuit to control the switching between synchronous and envelope detectors. This will prodoce a chattering effect unless hysteresis or a blend circuit is used. Think of this as semi synchronous detection with auto-blend without the complexity.

The maximum audio bandwidth is defined only by the RF/IF bandpasses but selectivity is defined by the very narrow bandwidth regenerative amp which drives the product detector. This is akin to using synchronous detection in which the BFO for the detector defines the relationship to the sideband energy and which the adjacent channel signal's detected output is also defined and not in relation to its own carrier if it should be stronger after being bandpass filtered. Unlike synchronous detection which requires a PLL and lock detection circuits to eliminate squeel when not locked onto the signal, this setup provides a natural tuning response not unlike that of an envelope detector without most of the pitfalls. It may even have a minor mute effect in between channels. As long as the narrowband filtered signal which drives the switching of the product detector is of sufficient level no amplitude modulation will effect detection as long as the detector is switched hard. If the bandwidth of the RegenerationQ & LoadedTankQ combined is 300Hz then the highest modulation frequency of the BFO in both amplitude and phase is 150Hz then this is within an area of the carrier that is fairly well protected. Removing most energy from the sidebands means that amplitude modulation is greatly reduced to the point where the switching of the detector will never invert under almost all conditions when the incoming signal is 100% modulated. This also virtually eliminates any phase produced by sideband assymetry or adjacent channel interfetence except for around 10kHz modulation of the adjacent signal which are mostly short transient bursts.

Co-channel interference producing a capture effect of the detector overriding the carrier of the desired signal is possible but this is also true for a PLL used for synchronous detection but a PLL is more immune to chattering between the two carriers. The chatter effect produced is probably similar to an FM detector when two signals are competing for capture in which the hysteresis is determined by its protection ratio. It won't switch between the two signals like FM but both signals will be detected and only the one in which carrier has captured the detector will be clear while the other would sound like an SSB signal with a poorly adjusted clairifier. Since a PLL's frequency is controlled by the loop amp its immunuty can be greater. A carrier's incidential co-channel phase modulation of ±8° whould only produce a cosine modulation of 1% or <0.1dB, mostly noticeable. As long as the AGC maintains a strong input level to the detector's BFO input the switching will remain hard removing any amplitude modulation. When the AGC range is exausted and as the signal level greatly fades in strength this will provide a natural blend to mute and thus an automatic gating effect for the blend.

The regeneration amp is based on a Hartley oscillator that is not quite at critical fedback. In most regeneration receivers the feedback control is adjusted to the point just prior to critical feedback. Exceeding this will result in a free running oscillator that may or may not stay synced to the signal. Aiming for ~97½% feedback is probably reasonable and that relates to a multiplication factor of 40. Above a factor of 50 or 98% the potential for self oscillation increases. An increase above 50 does not gain much more in selectivity in relation to reducing the stability for varying conditions that may induce critical feedback. 1% resistors are used in critical areas since larger tolerances may not hit the target within the feedback resistor's desired adjustment range. Using the feedback resistor as the primary adjustment mechanism provides both Q control and output level adjustment however having the idle current flow through the adjustment trimmer and bias resistor is not recomended. Instead use a resistor at least one size larger than recommended and parallel it up with a larger resistor to obtain the right value. Use a trimmer as the larger value to determine the size needed and then replace it with the correct fixed value. Having Tap2 set at 85% of Tap1 allows the use of a larger feedback resistor which reduces the effect that r'e has on feedback levels and also allows easy setting of the idle current. The resonant tank uses an Amidon ferrite torroid core material #61 which is high Q and temperature stable although other materials or pre-made coils could be used. Although the datasheet on it does not specify the actual Q or have any graphs like it does for the iron powder cores so an assumed Q of 150 is used. A Q of 1000 is used for the resonant capacitor resulting in a ~Q for the tank of 130. The actual inductor Q may be much different than what has been assumed but the higher the Q the better requiring less Q multiplication for the same bandwidth or a narrower bandwidth with the same multiplication factor. Winding with Litz wire will increase Q performance. The transistor bias load impedance on the tank is about equal to the tank itself at Tap1 (50%) and a variation of unloaded tank Q will affect levels but the feedback resistor adjustment should compensate for it. If the tank Q is much different than what has been used here then it maybe beneficial to change the bias resistors for input level or change the tap ratios to maximize available tank Q. The 2nd tank on the output delivers the signal to the MC1496 carrier port and provides bias for the inputs. For the MC1496 if the BFO is modulated the recommended input level is 300mVrms or ~850mVp-p. Specified in the drawing is the same tank used for the oscillator but a stock IFT could also be used. It provides a 2:1 transform reducing drive imedance by 4. This is also selective with an estimated bandwidth of ~10kHz providing minor improvement in selectively. Tuning of this tank can be used to trim the phase of the BFO to align it with the signal port input.

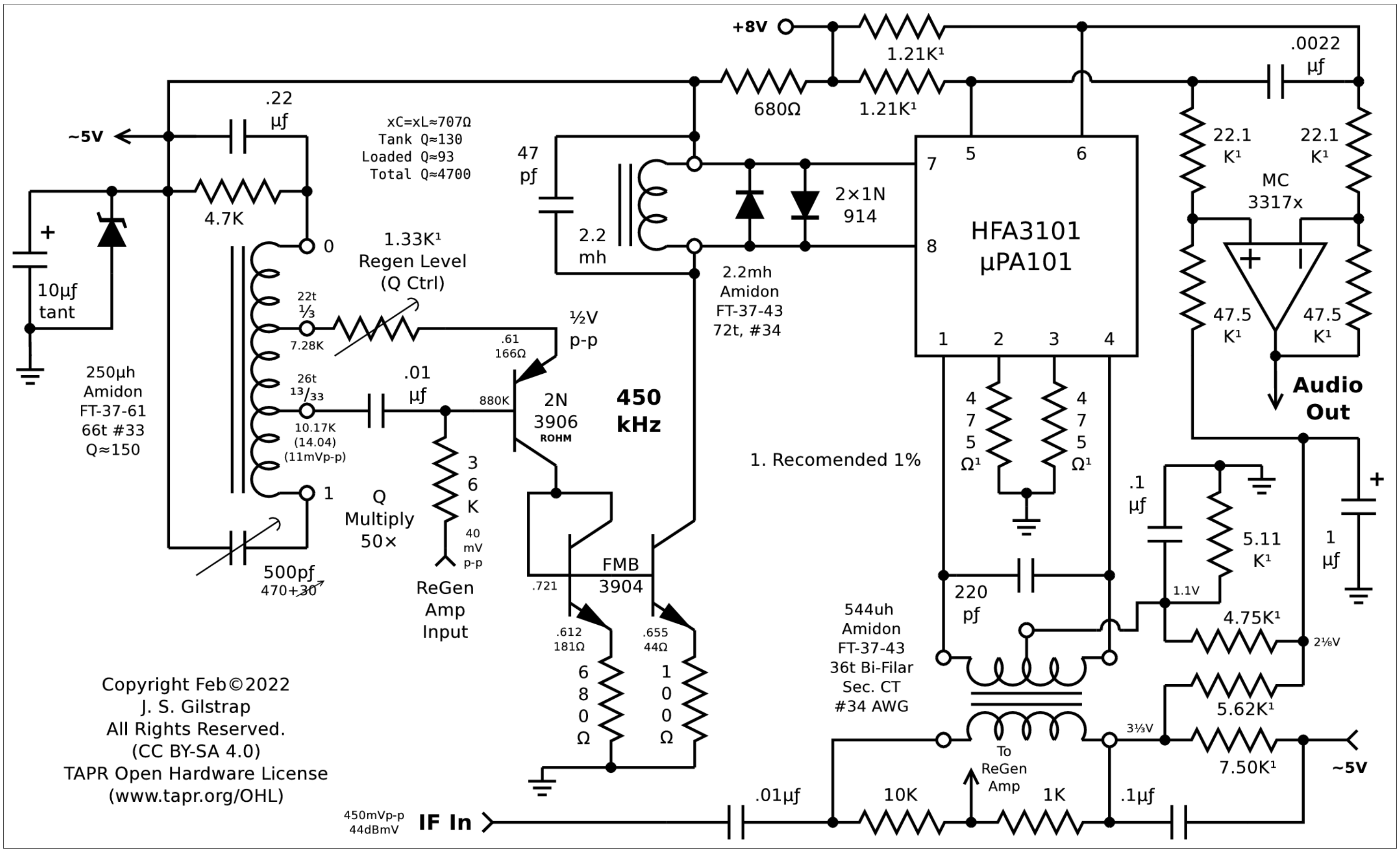
The input level to the circuit should be AGC controlled at an unmodulated level of 44dBmV or ~160mVrms and the drive source should be <1K.

Below is a spreadsheet output for the circuit as configued on page 2. It also has the cell formulas to recreate the sheet if desired. An xC & xL of 1K is hard coded into the spreadsheet formulas but a different value may prove more optimal for best performance. It can be used to calculate input and output levels, set tap ratios and idle current, operating Q levels, and other parameters for a different setup.

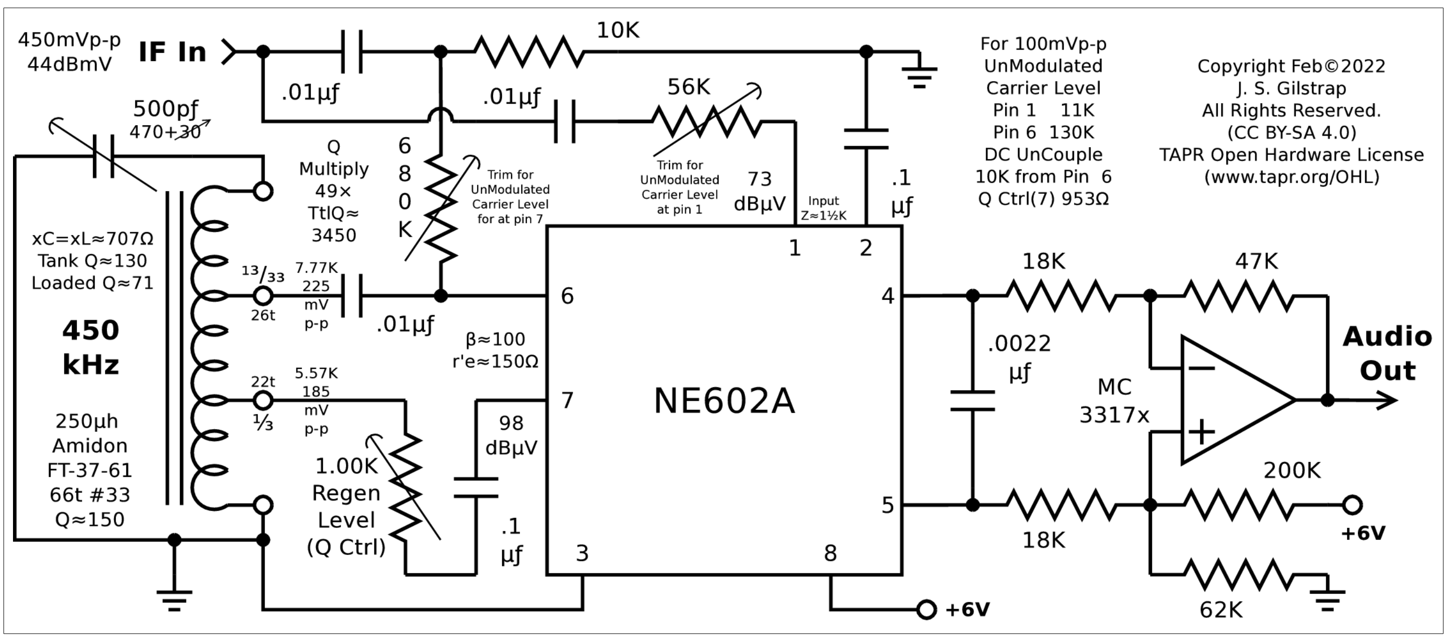
Calculation Spreadsheet

Given: Tank@455kHz xC=xL=1K Transistor: 2N3904 (25°C)					
	A	**B**	**C**	**Cell Equations**	
10	Input Level	**0.45**	Vp-p		
11	R in Network Bias	**4.5**	V	**Voltage @ Pin 4 of MC1496**	
12	R in 1	**130**	K		
13	R in 2	**47.5**	K	**Blue**	
14	2N3904 Re	**2.32**	K	**Values**	
15	Unloaded Tank Z	**130**	K (Q×X)	**are**	
16	Tap1	**0.5**	.%	**Input**	
17	Tap1:Tap2	**0.85**	.%	**Variables**	
18	Z @ 2N3904 Base	**2500**	K	β×(Re+r'e), β≈120	
19	Output Tank Z	**11**	K	Estimated	
20	2N3904 Vbe	**0.67**	V	Includes voltage drop induced by base load	
21	Tap1 Z autotrans	0.25	.%	=B16^2	
22	Tap1:Tap2 Z autotrans	0.7225	.%	=B17^2	
23	Tap1 Z wo/130K	19.149	K	=1/(1/(B15*B21)+1/B18+1/B13)	
24	Tap1 Z	16.691	K	=1/(1/B12+1/B23)	
25	Tap2 Z	12.059	K	=B22*B24	
26	Input Attenuation	0.128	.%	=1/(1+B12/B23)	
27	in @ Tap1	0.058	Vp-p	=B10*B26	
28	2N3904 Ve	0.534	V	=B11*B13/(B12+B13)-B20	
29	Idle Current	0.230	ma	=B28/B14	
30	r'e	0.126	K	=0.029/B29 r'e constant obtained from 2N3904 Vbe Log Graph	
31	Feedback	0.978	.%	=B25/(B14+B25+B30)/B17	
32	Loaded Tank Q	66.76		=B24/B21	
33	Gain Multiplier	45.7		=1/(1-B31)	
34	Out	2.638	Vp-p	=B27*B33	
35	dBmV	59.4		=20*log(500*B34/sqrt(2))	
36	Δi Out	0.182	ma	=B34/(B14+B25+B30)	
37	Output Tank V out	1.973	Vp-p	=B19*B36	
38	1496 Carrier Drive	0.987	Vp-p	=B37/2	2:1 Tap Ratio

This is another setup for 450kHz using lower supply voltage

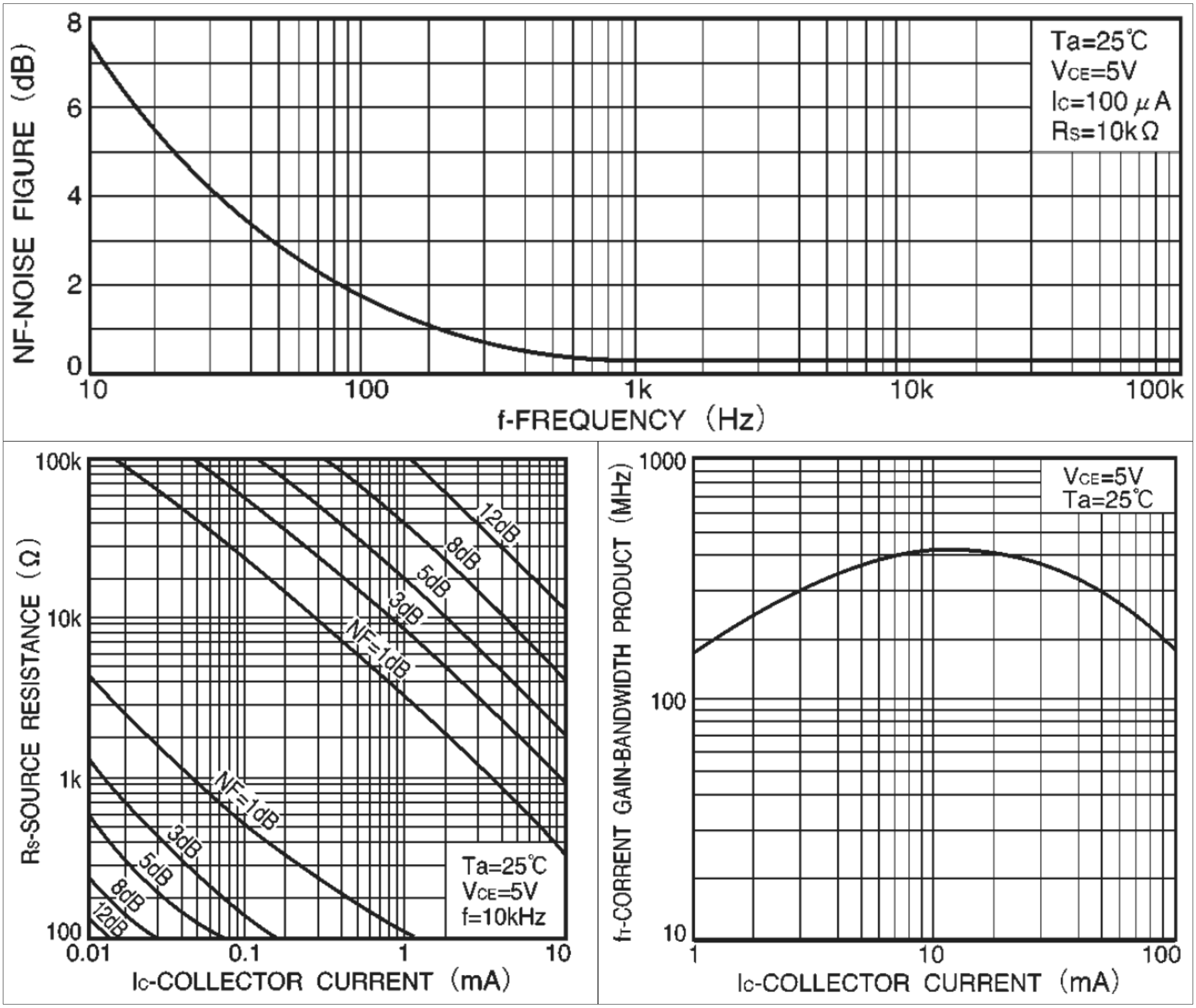


This uses a fully combined oscillator/detector IC for detection

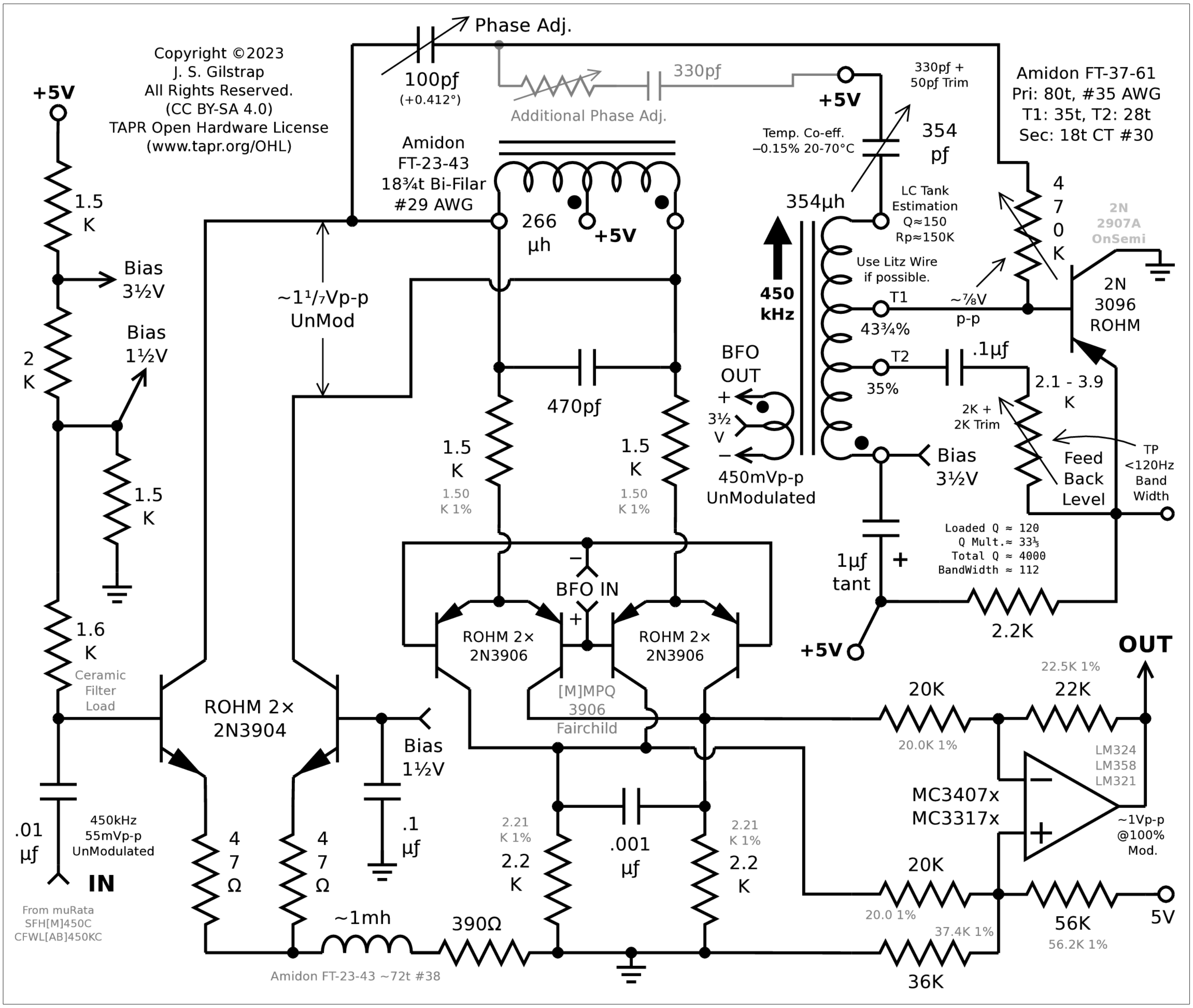


A potential variation could be to increase feedback till critical for synchronized oscillation once adequate signal level is reached. The blend would be completely transparent. It could be automatic in that the feedback level is directly coupled to detected signal level. This would basicly be full synchronous detection but with an appearant instant acquisition time.

For a general purpose BJT to be used in an oscillator the 2N2222A usually comes to mind but in the following graphs from the ROHM datasheet for the 2N3906 shows it too can be used if operated within range. It has lower capacitance, better Gain-Bandwidth Product at lower current levels, and its source resistance requirement is better optimized in this application. NF 3dB corner ≈ 45Hz & NF min ≈ ⅓dB, NF area ≈ 1dB, GBwP≈35MHz@150µa.



Discrete Component QuasiSync Detector



While a quad 2N3906 setup is used for the product detector as a switch and probably doesn't have the switching speed of a MC1496 it should perform adequately as rise and fall times at the collector outputs only need to support the audio frequency range as the rectified IF frequency will be filtered out. This leaves the transistors only need is to switch currents. The transistors are not driven into saturation so storage time is not an issue and rise and fall times at audio frequencies aren't either so the only factor left is the the turn on time at 35ns. Given that the turn off time is not specified using the turn on time for for turn off time for a switching time of 70ns may be reasonable estimate. Using this the switching time is only ~3% of the period. If faster switching times are desired using 4×MPSH81 will remedy this. The signal from the regeneration amp driving the transistors' bases should be in phase (0°) with the signal driving the 1.5K emitter resistors. If not phase adjustments can be made by adjusting the value of the 100pf input capacitor. If not enough range can be obtained from this without the capacitor getting too small and additional AC grounded loading resistor can be applied to the capacitor to induce more phase advance.